

# Microcomputer Technical Information

CP(K), O

|                                    |                                                                                                         |                             |                                                                                                                                   |                       |
|------------------------------------|---------------------------------------------------------------------------------------------------------|-----------------------------|-----------------------------------------------------------------------------------------------------------------------------------|-----------------------|
| V850/SF1<br><br>Usage Restrictions |                                                                                                         | Document No.                | ZBG-BF-05-0001                                                                                                                    | 1/2                   |
|                                    |                                                                                                         | Date issued                 | January 21, 2005                                                                                                                  |                       |
|                                    |                                                                                                         | Issued by                   | Car Audio Solution Development Group<br>Automotive Systems Division<br>4th Systems Operations Unit<br>NEC Electronics Corporation |                       |
| Related documents                  | V850/SF1 Hardware User's Manual: U14665EJ4V0UD<br>V850 Family Architecture User's Manual: U10243EJ7V0UD | Notification classification | √                                                                                                                                 | Usage restriction     |
|                                    |                                                                                                         |                             |                                                                                                                                   | Upgrade               |
|                                    |                                                                                                         |                             |                                                                                                                                   | Document modification |
|                                    |                                                                                                         |                             |                                                                                                                                   | Other notification    |

## 1. Affected products

V850/SF1 Series on-chip flash memory microcontrollers

μPD70F3079YGC

μPD70F3079AYGC, μPD70F703079AYGF

μPD70F3079AYGC(A)

## 2. Details of bug

This notification concerns the following bug (No. 8). See attachment 1 for details.

- No. 8 Bug related to the conflict between writing to external memory area and acknowledgement of bus hold request

## 3. Workaround

- No. 8 There is no workaround.

## 4. Action

The circuit will be modified to correct this bug.

| Part Number After Modification<br>(B Version) | Sample Shipment Schedule |                   |
|-----------------------------------------------|--------------------------|-------------------|
|                                               | ES                       | CS                |
| μPD70F3079BYGC-8EU                            | Late January, 2005       | Early April, 2005 |
| μPD70F3079BYGF-3BA                            |                          |                   |
| μPD70F3079BYGC(A)-8EU                         |                          |                   |

\* For the detailed release schedule of modified products, contact an NEC Electronics sales representative.

5. Document revision history

| Document Number | Issued on         | Description                                      |
|-----------------|-------------------|--------------------------------------------------|
| SBG-DT-0008     | October 4, 2001   | Newly created. Addition of bugs (No. 1 to No. 5) |
| SBG-DT-02-0028  | December 12, 2002 | Addition of bugs (No. 6 and No. 7)               |
| ZBG-BF-05-0001  | January 21, 2005  | Addition of bug (No. 8)                          |

6. List of restrictions

A list of restrictions in the V850/SF1, including the revision history and detailed information, is described on the following pages.

## List of Restrictions in V850/SF1

### 1. Product Version

- V850/SF1 (B version)  
 $\mu$ PD70F3079BYGC/GF,  $\mu$ PD70F3079BYGC(A): Rank K
- V850/SF1 (A version)  
 $\mu$ PD703075AYGC/GF,  $\mu$ PD703075AYGC(A): Rank K  
 $\mu$ PD703076AYGC/GF,  $\mu$ PD703076AYGC(A): Rank K  
 $\mu$ PD703078AYGC/GF,  $\mu$ PD703078AYGC(A): Rank K  
 $\mu$ PD703079AYGC/GF,  $\mu$ PD703079AYGC(A): Rank K  
 $\mu$ PD70F3079AYGC/GF,  $\mu$ PD70F3079AYGC(A): Rank K
- V850/SF1  
 $\mu$ PD703078YGC/GF: Rank K, E  
 $\mu$ PD703079YGC/GF: Rank K, E  
 $\mu$ PD70F3079YGC/GF: Rank K, E

\* The rank is indicated by the letter appearing as the 5th digit from the left in the lot number marked on each product.

### 2. Product History

V850/SF1 B versions (flash memory versions):  $\mu$ PD70F3079BY,  $\mu$ PD70F3079BY(A)

| No. | Bugs and Restrictions                                                                                       | Rank     |
|-----|-------------------------------------------------------------------------------------------------------------|----------|
|     |                                                                                                             | K        |
| 1   | FCAN global timer clock selection                                                                           | –        |
| 2   | Restriction on 16-bit timer one-shot pulse output function                                                  | $\Delta$ |
| 3   | Restriction on interrupt servicing acknowledgement after EI instruction                                     | $\Delta$ |
| 4   | External bus interface address incrementation                                                               | –        |
| 5   | Restriction on power save function on external ROM                                                          | $\Delta$ |
| 6   | Restriction on reading the ISPR register                                                                    | $\Delta$ |
| 7   | Restriction on rewriting compare values during 16-bit timer (TM2 to TM6) count operation                    | $\Delta$ |
| 8   | Bug related to the conflict between writing to external memory area and acknowledgement of bus hold request | $\surd$  |

$\surd$ : Bug does not occur,  $\Delta$ : Bug will also apply in future,  $\times$ : Bug occurs, –: Not relevant

V850/SF1 A versions (mask ROM versions):

$\mu$ PD703075AY,  $\mu$ PD703076AY,  $\mu$ PD703078AY,  $\mu$ PD703079AY,  
 $\mu$ PD703075AY(A),  $\mu$ PD703076AY(A),  $\mu$ PD703078AY(A),  $\mu$ PD703079AY(A)

| No. | Bugs and Restrictions                                                                                       | Rank     |
|-----|-------------------------------------------------------------------------------------------------------------|----------|
|     |                                                                                                             | K        |
| 1   | FCAN global timer clock selection                                                                           | –        |
| 2   | Restriction on 16-bit timer one-shot pulse output function                                                  | $\Delta$ |
| 3   | Restriction on interrupt servicing acknowledgement after EI instruction                                     | $\Delta$ |
| 4   | External bus interface address incrementation                                                               | –        |
| 5   | Restriction on power save function on external ROM                                                          | $\Delta$ |
| 6   | Restriction on reading the ISPR register                                                                    | $\Delta$ |
| 7   | Restriction on rewriting compare values during 16-bit timer (TM2 to TM6) count operation                    | $\Delta$ |
| 8   | Bug related to the conflict between writing to external memory area and acknowledgement of bus hold request | –        |

√: Bug does not occur,  $\Delta$ : Bug will also apply in future,  $\times$ : Bug occurs, –: Not relevant

V850/SF1 A versions (flash memory versions):  $\mu$ PD70F3079AY,  $\mu$ PD70F3079AY(A)

| No. | Bugs and Restrictions                                                                                       | Rank     |
|-----|-------------------------------------------------------------------------------------------------------------|----------|
|     |                                                                                                             | K        |
| 1   | FCAN global timer clock selection                                                                           | –        |
| 2   | Restriction on 16-bit timer one-shot pulse output function                                                  | $\Delta$ |
| 3   | Restriction on interrupt servicing acknowledgement after EI instruction                                     | $\Delta$ |
| 4   | External bus interface address incrementation                                                               | –        |
| 5   | Restriction on power save function on external ROM                                                          | $\Delta$ |
| 6   | Restriction on reading the ISPR register                                                                    | $\Delta$ |
| 7   | Restriction on rewriting compare values during 16-bit timer (TM2 to TM6) count operation                    | $\Delta$ |
| 8   | Bug related to the conflict between writing to external memory area and acknowledgement of bus hold request | $\Delta$ |

√: Bug does not occur,  $\Delta$ : Bug will also apply in future,  $\times$ : Bug occurs, –: Not relevant

V850/SF1 (mask ROM versions):  $\mu$ PD703078Y,  $\mu$ PD703079Y

| No. | Bugs and Restrictions                                                                                       | Rank     |          |
|-----|-------------------------------------------------------------------------------------------------------------|----------|----------|
|     |                                                                                                             | K        | E        |
| 1   | FCAN global timer clock selection                                                                           | –        | –        |
| 2   | Restriction on 16-bit timer one-shot pulse output function                                                  | $\Delta$ | $\Delta$ |
| 3   | Restriction on interrupt servicing acknowledgement after EI instruction                                     | $\Delta$ | $\Delta$ |
| 4   | External bus interface address incrementation                                                               | –        | –        |
| 5   | Restriction on power save function on external ROM                                                          | $\Delta$ | $\Delta$ |
| 6   | Restriction on reading the ISPR register                                                                    | $\Delta$ | $\Delta$ |
| 7   | Restriction on rewriting compare values during 16-bit timer (TM2 to TM6) count operation                    | $\Delta$ | $\Delta$ |
| 8   | Bug related to the conflict between writing to external memory area and acknowledgement of bus hold request | –        | –        |

✓: Bug does not occur,  $\Delta$ : Bug will also apply in future,  $\times$ : Bug occurs, –: Not relevant

V850/SF1 (flash memory version):  $\mu$ PD70F3079Y

| No. | Bugs and Restrictions                                                                                       | Rank     |          |
|-----|-------------------------------------------------------------------------------------------------------------|----------|----------|
|     |                                                                                                             | K        | E        |
| 1   | FCAN global timer clock selection                                                                           | $\times$ | ✓        |
| 2   | Restriction on 16-bit timer one-shot pulse output function                                                  | $\Delta$ | $\Delta$ |
| 3   | Restriction on interrupt servicing acknowledgement after EI instruction                                     | $\Delta$ | $\Delta$ |
| 4   | External bus interface address incrementation                                                               | $\times$ | ✓        |
| 5   | Restriction on power save function on external ROM                                                          | $\Delta$ | $\Delta$ |
| 6   | Restriction on reading the ISPR register                                                                    | $\Delta$ | $\Delta$ |
| 7   | Restriction on rewriting compare values during 16-bit timer (TM2 to TM6) count operation                    | $\Delta$ | $\Delta$ |
| 8   | Bug related to the conflict between writing to external memory area and acknowledgement of bus hold request | $\Delta$ | $\Delta$ |

✓: Bug does not occur,  $\Delta$ : Bug will also apply in future,  $\times$ : Bug occurs, –: Not relevant

### 3. Details of Usage Restrictions

#### No. 1 FCAN global timer clock selection

##### [Description]

Because the global timer clock selection, which is set using the GTCS1 and GTCS0 bits of the CGCS register, cannot be set, it is fixed to the initial value  $f_{GTS1} = f_{MEM}/2$ .  $f_{MEM}/4$ ,  $f_{MEM}/8$  and  $f_{MEM}/16$  cannot be set.

#### No. 2 16-bit timer one-shot pulse output function

##### [Description]

When using the one-shot pulse function of timers 0, 1, and 7 as a software trigger, the level of the T1 pin or its alternate function port cannot be changed.

Because the external trigger is also enabled in this case, the trigger will inadvertently clear & start even if the level of the T1 pin or its alternate function port is changed, causing a pulse to be output at an unintended timing.

#### No. 3 Interrupt servicing acknowledgement after EI instruction

##### [Description]

In this product, at least 7 clocks are required as determination time between the generation of an interrupt and its acknowledgement. Because instructions continue to be executed in this period, if the DI instruction (interrupt disable) is executed, interrupts become disabled. This causes all interrupts to be held pending until the re-execution of the EI instruction (interrupt enable).

Since this determination time is also required when the EI instruction is executed, at least 7 clocks must be allowed before interrupts can be acknowledged after execution of the EI instruction. Consequently, if the DI instruction is executed before these 7 clocks have elapsed, interrupts will be held pending and not acknowledged.

To ensure proper acknowledgement of interrupts therefore, insert an instruction (other than those below) of at least 7 execution clocks between the EI and DI instructions.

- IDLE/STOP mode setting
- EI, DI instruction
- RETI instruction
- LDSR instruction (for PSW register)
- Access to interrupt control register (xxICn)

Example: When EI instruction processing is invalid

##### [Program example]

```

DI
:           ; MK flag = 0 (interrupts enabled)
:           ; Interrupt request generated (IF flag = 1)
EI
JR LP1
:           ; 7 clocks have not elapsed between EI and DI instructions (3 clocks)
:
LP1:
DI         ← ; Interrupt request is not acknowledged.
:

```

## [Workaround example]

```

DI
:           ; MK flag = 0 (interrupts enabled)
:           ; Interrupt request generated (IF flag = 1)
EI
NOP         ; 1 system clock
NOP         ; 1 system clock
NOP         ; 1 system clock
NOP         ; 1 system clock
JR  LP      ; 3 system clocks (branch to LP1 routine)
:
LP1:
DI          ← ; Interrupt servicing is executed at 8th clock cycle after the EI instruction
:

```

## No. 4 External bus interface address incrementation

## [Description]

When the external bus interface is used and the address bus A16 to A21 is incremented, an address value 10000H larger than the expected value is inadvertently output for the address immediately before it was incremented.

For example, if the address value is incremented from 14FFFEH to 150000H, the erroneous address 15FFFEH is output at the timing at which 14FFFEH should be output.

## [Cause of bug]

The clock signal that latches the address bus data A16 to A21 is delayed beyond the internal address bus data change point by the circuit added to enable support of the EVA chip function, which causes the address value of the next bus cycle to be latched.

A detailed timing chart is provided on the attachment.

Note that because the EVA chip function circuit is only incorporated in flash memory products, this bug does not occur in mask ROM products.

## [Workaround]

## (i) Temporary workaround

Using software, make the address area in which the address bus A21 to A16 is incremented use-prohibited when using the external bus interface.

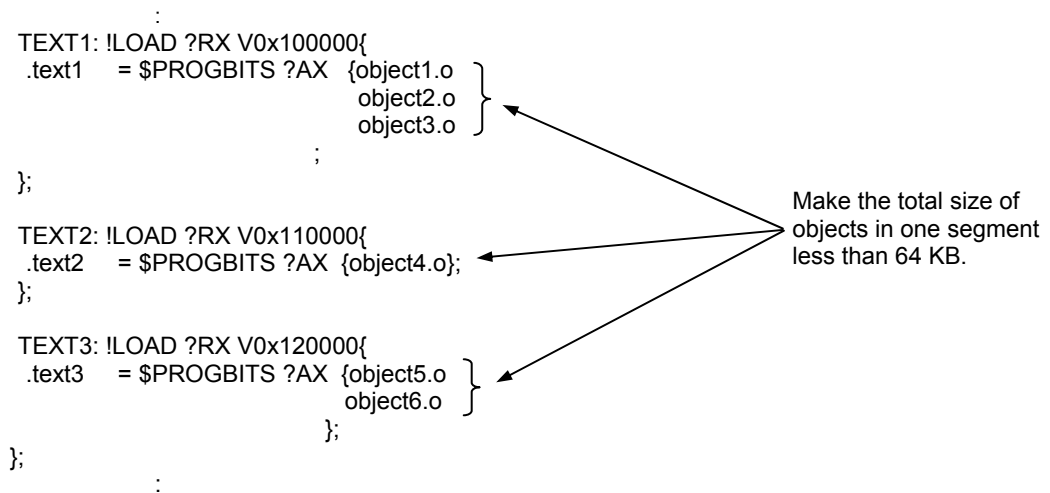
## • Use-prohibited area

xxnmFFF8H to xxnmFFFFEH (n = 0 to 3, m = 0 to E)

xxnFFFF8H to xxnFFFFEH (n = 0 to 2)

- Example of workaround

Using a link directive file, ensure that program code is not allocated to the use-prohibited area described above.



## No. 5 Power save function on external ROM

### [Description]

If the affected products are used under the following conditions, a discrepancy may occur between the address indicated by the program counter (PC) and the address at which the instruction is actually read following the release of a power save mode.

This may result in the CPU ignoring a 4- or 8-byte instruction from between 4 bytes and 16 bytes after an instruction is executed to write to the PSC register, which could in turn result in the execution of an erroneous instruction. Note that this bug only occurs if all of conditions (1) to (3) below are met.

### [Conditions]

- (1) A power save mode (IDLE or STOP) is set while an instruction is being executed on the external ROM.
- (2) The power save mode is released by an interrupt.
- (3) The next instruction is executed while interrupts are in a pending state following the release of the power save mode.

Note that interrupts are held pending under any of the following conditions.

- <1> The NP flag of the PSW register is 1. (NMI servicing in progress/set by software)
- <2> The ID flag of the PSW register is 1. (Interrupt servicing in progress/DI instruction/set by software)
- <3> The EI (interrupt enable) state had been set during interrupt servicing to enable multiple interrupt servicing, but was released by an interrupt with the same or lower priority than the interrupt being serviced.

The operation of the bug is shown below using the power save mode setting example from the user's manual.

(rD: PSC setting value, rX: Value written to PSW, rY: Value written back to PSW, assuming PSW has been set)

|                    |                               |                  |
|--------------------|-------------------------------|------------------|
| ldsr rX,5          | ; Sets PSW to the value of rX |                  |
| st.b r0,PRCMD[r0]  | ; Writes to PRCMD             |                  |
| st.b rD,PSC[r0]    | ; Sets the PSC register       | (PSC setting)    |
| ldsr rY,5          | ; Returns the value of PSW    | (After 4 bytes)  |
| nop                | ; 2 to 5 NOP instructions     | (After 6 bytes)  |
| nop                | ;                             | (After 8 bytes)  |
| nop                | ;                             | (After 10 bytes) |
| nop                | ;                             | (After 12 bytes) |
| nop                | ;                             | (After 14 bytes) |
| (Next instruction) | ;                             | (After 16 bytes) |

} Bug occurs here  
 <1>Discrepancy with PC  
 <2>Instructions ignored

## [Workaround]

- (1) Do not use a power save mode (IDLE or STOP) while an instruction is being executed on the external ROM.
- (2) If it is necessary to use a power save mode (IDLE or STOP) while an instruction is being executed on the external ROM, take the software workaround shown below.
  - <1> Insert 6 NOP instructions 4 bytes after an instruction that writes to the PSC register.
  - <2> Insert the br \$+2 instruction after the NOP instructions to eliminate the PC discrepancy.

## [Program example]

(rD: PSC setting value, rX: Value written to PSW, rY: Value written back to PSW, assuming PSW has been set)

|                   |                                  |
|-------------------|----------------------------------|
| ldsr rX,5         | ; Sets PSW to the value of rX    |
| st.b r0,PRCMD[r0] | ; Writes to PRCMD                |
| st.b rD,PSC[r0]   | ; Sets the PSC register          |
| ldsr rY,5         | ; Returns the value of PSW       |
|                   |                                  |
| nop               | ; <1> 6 or more NOP instructions |
| nop               |                                  |
| nop               |                                  |
| nop               |                                  |
| nop               |                                  |
| nop               |                                  |
| br \$+2           | ; <2> Eliminates PC discrepancy  |

## No. 6 Restriction on reading the ISPR register

## [Description]

When an interrupt request to the CPU is generated from INTC, the CPU returns the interrupt ACK signal to INTC if the request is acknowledgeable and enters the interrupt service routine after the instruction currently being executed is complete. When the interrupt ACK signal is received, INTC sets the ISPR register. This processing in INTC is performed asynchronously to the CPU.

If the following three conditions conflict, therefore, the value after ISPR is set may be read even though the CPU still has not entered the interrupt service routine.

- (1) CPU executes a load instruction to the ISPR flag
- (2) An interrupt request to the CPU occurs while the instruction in (1) is being executed
- (3) DMA transfer occurs while the instruction in (1) is being executed

At this time, the CPU jumps to the interrupt service routine as soon as the instruction execution in (1) is complete. However, the instruction execution in (1) is delayed due to DMA transfer in (3). The CPU acknowledges the interrupt request in (2) during this period and returns the ACK signal to INTC, and the ISPR flag is set before the read timing of (1).

[Workaround]

Read the ISPR register while interrupts are disabled (DI state).

No. 7 Restriction on rewriting compare values during 16-bit timer (TM2 to TM6) count operation

[Description]

The higher 8 bits of the CRn register are undefined when the value of the compare register (CRn: n = 2 to 6) is changed during a timer count operation.

[Workaround]

Be sure to stop the timer count operation before setting values to the compare register (CRn: n = 2 to 6).

No. 8 Bug related to the conflict between writing to external memory area and acknowledgement of bus hold request

[Description]

If a write operation (R/W signal = L) to the external memory area and acknowledgement of a bus hold request (HLDRQ) conflict at a specific timing, the R/W signal becomes the high level (read) though it is in the write cycle.

Consequently, the write operation to the external memory area cannot be performed normally in the bus cycle in which the conflict has occurred.

[Workaround]

There is no workaround.

[Action]

The circuit will be modified to correct this bug.

[Part number after modification (B version)]

μPD70F3079BYGC-8EU

μPD70F3079BYGF-3BA

μPD70F3079BYGC(A)-8EU

## Cautions

(1) Implement the following procedure when the debugger is activated when emulating the FCAN function using the emulation board (IE-703079-MC-EMI).

- a) Supply power to the VDD0 pin (GC package: pin 8, GF package: pin 11) from the target board before the debugger is activated.
- b) Set the memory mapping in the debugger as shown below.

Attribute: Target memory

Mapping address: nFF800H to nFFFFFFH (n = 3, 7, or B)

- c) Do not mask WAIT and HLDRQ when accessing the FCAN memory.



| DCLK1 | DCLK0 | Specification of CLKOUT Pin Operation                                           |
|-------|-------|---------------------------------------------------------------------------------|
| 0     | 0     | Output enabled                                                                  |
| 0     | 1     | V850/SF1: Setting prohibited<br>V850/SF1 A version: Hi-Z output <sup>Note</sup> |
| 1     | 0     | Setting prohibited                                                              |
| 1     | 1     | Output disabled (low-level output)                                              |

**Note** Hi-Z output is not possible in the in-circuit emulator.

<2> Modification of CLKOUT pin status during reset period

|                    |                                                                     |
|--------------------|---------------------------------------------------------------------|
| V850/SF1           | Hi-Z                                                                |
| V850/SF1 A version | Low level (insertion of pull-down resistor) <sup>Note 1, 2, 3</sup> |

**Notes 1.** A pull-down resistor can be inserted during the reset period only.

The setting is changed to low-level output (default setting of the PSC register) when a reset is released.

2. Do not input a high level to the CLKOUT pin when reset is released; otherwise the operation after the input cannot be guaranteed.
3. Pull-down resistor value: 40 kΩ TYP.

(3) Modification of the FCAN time stamp function specification

The value of the time stamp counter is not captured even if EOF is detected in the CAN bus.

Modification of settings of the TMR bit of the CANn control register (CnCTRL)

| TMR | Time Stamp Control Bit for Reception                                                                                                                                                         |
|-----|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0   | V850/SF1: The value of the time stamp counter is captured when an EOF is detected (confirms the valid message) in the CAN bus.<br>V850/SF1 A version: The time stamp counter is not captured |
| 1   | The value of the time stamp counter is captured when an EOF is detected (confirms the valid message) in the CAN bus.                                                                         |

(4) Expansion of operating voltage range at 16 MHz operation

|                    | Flash Memory Version @ 16 MHz | Mask ROM Version @ 16 MHz |
|--------------------|-------------------------------|---------------------------|
| V850/SF1           | 4.5 to 5.5 V                  | 4.0 to 5.5 V              |
| V850/SF1 A version | 4.0 to 5.5 V                  | 3.5 to 5.5 V              |

Other electrical specifications have been modified.

In particular, the AC characteristics have been modified, but this is modification in line with the above voltage range expansion. Therefore, there is no problem in upgrading from a previous version of the V850/SF1 to an A version of the V850/SF1.

Refer to the electrical specifications chapter in the user's manual.

(5) Addition of mask ROM 128 KB version to product lineup

μPD703076AY ROM: 128 KB, RAM: 12 KB, FCAN: 2 channels

μPD703075AY ROM: 128 KB, RAM: 12 KB, FCAN: 1 channel